REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correction to table I differential nonlinearity test limit. Editorial changes throughout. - drw	00-08-25	Raymond Monnin
B	Update drawing to current requirements. – drw	06-08-30	Raymond Monnin

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B				
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11				

PMIC N/A

PREPARED BY
Sandra Rooney

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Sandra Rooney

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
94-01-20

REVISION LEVEL
B

MICROCIRCUIT, LINEAR, 12-BIT SERIAL DACPORT, MONOLITHIC SILICON

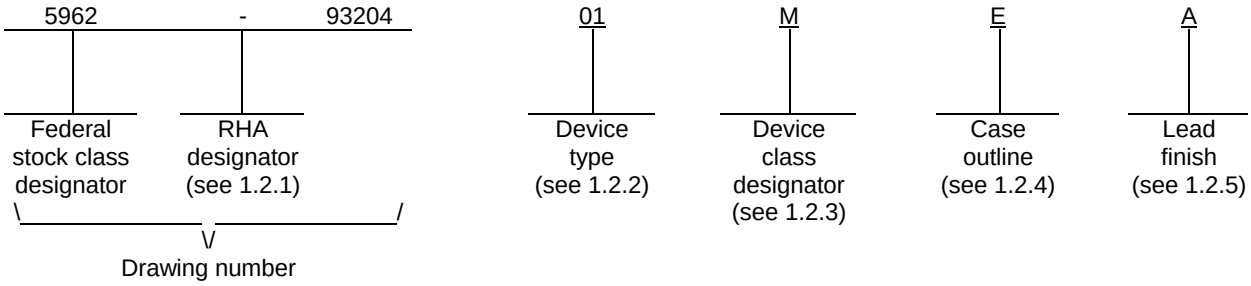
SIZE	CAGE CODE	
A	**67268**	**5962-93204**

SHEET 1 OF 11

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	AD7243	12-bit serial DACPORT

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outline is as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/,2/

V_{DD} to AGND, DGND	-0.3 V dc to +17 V dc
V_{SS} to AGND, DGND	+0.3 V dc to -17 V dc
AGND to DGND	-0.3 V dc to V_{DD} + 0.3 V dc
V_{OUT} to AGND 3/	-6 V dc to V_{DD} + 0.3 V dc
REFOUT to AGND	0 V dc to V_{DD}
REFIN to AGND	-0.3 V dc to V_{DD} + 0.3 V dc
Digital inputs to DGND	-0.3 V dc to V_{DD} + 0.3 V dc
SDO to DGND	-0.3 V dc to V_{DD} + 0.3 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation (P_D) (T_A = +75°C) 4/	450 mW

1.4 Recommended operating conditions.

Positive supply voltage range (V_{DD})	+12 V dc to +15 V dc 5/
Negative supply voltage range (V_{SS})	0 V dc or -12 V dc to -15 V dc 5/
Voltage reference input (REFIN)	+5 V dc
Ambient operating temperature range	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ T_A = +25°C unless otherwise specified.
3/ The outputs may be shorted to voltages in this range provided the power dissipation of the package is as specified. Short circuit current is typically 80 mA.
4/ Derate power dissipation above T_A = +75°C by 6 mW/°C.
5/ Power supply tolerance ±5%.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 80 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Relative accuracy 2/	RA		1, 2, 3	01		±1	LSB
Differential nonlinearity 2/	DNL	Guaranteed monotonic	1, 2, 3	01		±0.9	LSB
Unipolar offset error 2/	UOE	DAC latch contents all 0s	1, 2, 3	01		±5	LSB
Bipolar zero error	BZE	DAC latch contents 2048	1, 2, 3	01		±6	LSB
Full scale error 2/ 3/	AE		1, 2, 3	01		±7	LSB
Voltage reference output	REFOUT		1, 2, 3	01	4.95	5.05	V
Reference load change	REFLC	Reference load current (I_L) change (0-100 μA)	1, 2, 3	01		-1	mV
Reference input range 4/	REFIN		1, 2, 3	01	4.95	5.05	V
Reference input current	RIN		1, 2, 3	01		5	μA
Digital input high voltage 2/	V_{INH}		7. 8	01	2.4		V
Digital input low voltage 2/	V_{INL}		7, 8	01		0.8	V
Digital input current	I_{IN}	V_{IN} = 0 V to V_{DD}, V_{DD} = 15.75 V, V_{SS} = -15.75 V	1, 2, 3	01		±1	μA
Input capacitance	C_{IN}	See 4.4.1c	4	01		8	pF
Digital output low voltage	V_{OL}	I_{SINK} = 1 mA	1, 2, 3	01		0.4	V
Digital output high voltage	V_{OH}	I_{SOURCE} = 400 μA	1, 2, 3	01	4.0		V
Analog output range resistor	R_{OUT}		1, 2, 3	01	15	30	kΩ
Analog output voltage ranges 5/	V_{OUT}	Single supply, V_{SS} = 0 V	1, 2, 3	01	5	10	V
		Dual supplies, V_{SS} = -12 V to -15 V			5 -5	10 +5	
Positive power supply current	I_{DD}	V_{DD} = 15.75 V, V_{SS} = -15.75 V, output unloaded, 10 V range	1, 2, 3	01		12	mA
Negative power supply current	I_{SS}	V_{DD} = 15.75 V, V_{SS} = -15.75 V, output unloaded, 10 V range, dual supplies	1, 2, 3	01		4	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Voltage output settling time, positive full scale 6/ change	t_{PS}	See 4.4.1c	4	01		12	µs
Voltage output settling time, negative full scale 6/ change	t_{NS}	V_{SS} = -12 V to -15 V See 4.4.1c	4	01		10	µs
SCLK cycle time 7/ 8/	t_1	SCLK mark/space ratio range is 40/60 to 60/40, see figure 2	9, 10, 11	01	200		ns
$\overline{\text{SYNC}}$ to SCLK falling edge setup time 7/ 8/	t_2	See figure 2	9, 10, 11	01	50		ns
$\overline{\text{SYNC}}$ to SCLK hold time 7/ 8/	t_3	See figure 2	9	01	120		ns
			10, 11		190		
Data setup time 7/ 8/	t_4	See figure 2	9, 10, 11	01	10		ns
Data hold time 7/ 8/	t_4	See figure 2	9, 10, 11	01	100		ns
$\overline{\text{SYNC}}$ high to $\overline{\text{LDAC}}$ low 7/ 8/	t_6	See figure 2	9, 10, 11	01	0		ns
$\overline{\text{LDAC}}$ pulse width 7/ 8/	t_7	See figure 2	9, 10, 11	01	50		ns
$\overline{\text{LDAC}}$ high to $\overline{\text{SYNC}}$ low 7/ 8/	t_6	See figure 2	9, 10, 11	01	0		ns
$\overline{\text{CLR}}$ pulse width 7/ 8/	t_9	See figure 2	9, 10, 11	01	75		ns
SCLK falling edge to SD0	t_{10}	SD0 load capacitance is no	9	01		120	ns
Valid 7/ 8/ 9/		Greater than 50 pF	10, 11			180	

1/ V_{DD} = +11.4 V to +15.75 V. V_{SS} = 0 V or –11.4 V to –15.75 V. AGND = DGND = 0 V. REFIN = +5 V. R_L = 2 kΩ. C_L = 100 pF to AGND. Parts are guaranteed over this supply range. Individual tests are performed with known worst case supply conditions. Unless otherwise noted V_{DD} = +11.4 V and V_{SS} = –11.4 V

2/ V_{DD} = 14.25 V, V_{SS} = 0 V on 10 V range. V_{DD} = 14.25 V, V_{SS} = –14.25 V on 10 V range. V_{DD} = 11.4 V, V_{SS} = –11.4 V on 5 V range

3/ Measured with respect to REFIN and includes unipolar and bipolar offset error.

4/ REFIN is connected to REFOUT for all tests except R_{IN}.

5/ Analog output voltage ranges are guaranteed by passing of DC accuracy tests.

6/ 0 V to +10 V output range is available only with $V_{DD} \ge +14.25$ V.

7/ All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% 0f 5 V) and timed from a voltage level of 1.6 V.

8/ Subgroups 10 and 11 are measured only at initial design characterization and after process or design changes which might affect this parameter. This limit is guaranteed even though it is not tested.

9/ t_{10} measured only at initial design characterization and after process or design changes which might affect this parameter. This limit is guaranteed even though it is not tested.

Device type	01
Case outline	E
Terminal number	Terminal symbol
1	REFIN
2	REFOUT
3	$\overline{CLR}$
4	$\overline{BIN}$/COMP
5	SCLK
6	SDIN
7	$\overline{SYNC}$
8	DGND
9	$\overline{LDAC}$
10	DCEN
11	SD0
12	AGND
13	R_{OFS}
14	V_{OUT}
15	V_{SS}
16	V_{DD}

FIGURE 1. Terminal connections.

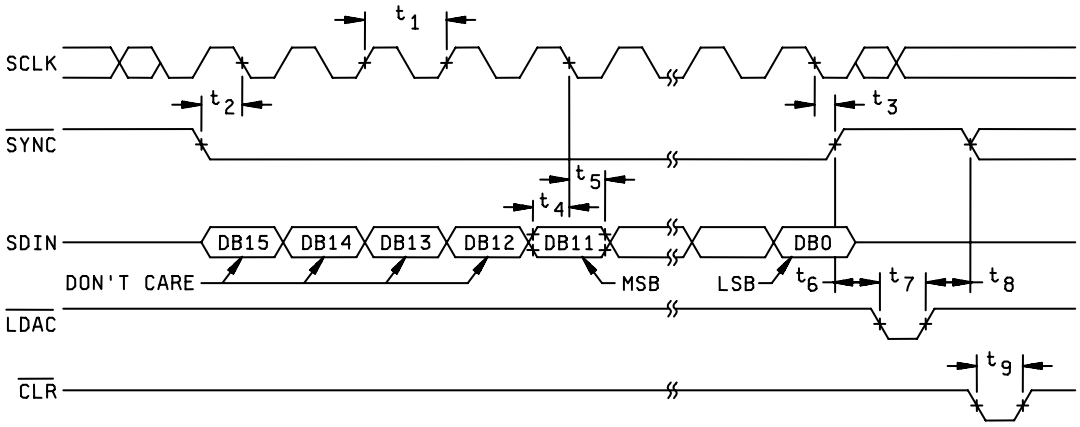


FIGURE 2. Timing waveforms.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 shall be measured only for initial qualification and after any process or design changes which may affect the parameter. Sample size is 15 devices with no failures, and all inputs tested.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7	1, 7	1, 7
Final electrical parameters (see 4.2)	1, 2, 3, 4, 7, 8, 9 1/	1, 2, 3, 4, 7, 8, 9 1/	1, 2, 3, 4, 7, 8, 9 1/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9	1, 2, 3, 4, 7, 8, 9	1, 2, 3, 4, 7, 8, 9
Group C end-point electrical parameters (see 4.4)	1	1	1, 2, 3, 4, 7, 8, 9
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	1	1	1

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-08-30

Approved sources of supply for SMD 5962-93204 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9320401MEA	24355	AD7243SQ/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: (35361)495999 Raheen Business Park Limerick, Ireland